Note: -
1.   **All questions are compulsory.**
2.   **Figures to the right indicate full marks.**
3.   **Students will be allowed 15 Minutes extra time per hour.**

PART B

Q.2 - Answer the Following - (Any 2 out of 4)   08 Marks
   1.   What are interrupts?
   2.   Explain the concept of address bus with diagram.
   3.   Draw and explain architecture of 8085 microprocessor.
   4.   Explain the concept of data bus for memory.

Q.3 - Answer the Following - (Any 2 out of 4)   08 Marks
   1.   Explain the MOV M, R instructions in brief
   2.   Explain the SUB M instructions in brief
   3.   Unpack the packed BCD register.
   4.   Write the assembly language program to find 1st complement.   **(P.T.O)**

Q.4 - Answer the Following - (Any 2 out of 4)   08 Marks
1. Write a program to calculate the sum of 8 bit numbers assuming sum to be 16 bits.
2. Write a program to sort numbers in ascending order.
3. Write a short note on subroutines.
4. Explain Nested subroutines with example.

Q.5 - Answer the Following - (Any 2 out of 4)   08 Marks
1. Write a program to convert Binary to BCD.
2. Explain the interrupt structure of 8085.
3. Explain the functional block diagram of 8155.
4. Explain the modes of the I/O ports of 8155.

Q.6 - Answer the Following - (Any 2 out of 4)   08 Marks
1. List the Pentium registers.
2. Write a note on addressing in real mode.
3. Explain the virtual mode of Pentium processor.
4. Explain the features of Pentium-4 processor.

Duration: - 2 ½ Hours]　　　　　**IT95MA22**　　　　　**[Marks 75]**

Note: -

1.　All questions are compulsory.
2.　Figures to the right indicate full marks.
3.　Students will be allowed 15 Minutes extra time per hour.

PART A

Q.1 Multiple Choice Questions　　　　　　　　35 Marks (1 Marks Each)

1. In 8085 microprocessor, the RST6 instruction transfer programme execution to following location
   a. 0030H　　b. 0024H　　c. 0048H　　d.0060H

2. HLT opcode means
   a. load data to accumulator　　b. store result in memory
   c. load accumulator with contents of register　d.end of program

3. What is SIM?　a) Select interrupt mask　　b.Sorting interrupt mask
   　　c. Set interrupt mask　d.Service interrupt machine

4. The ROM programmed during manufacturing process itself is called
   a. MROM　　b.PROM　　c.EPROM　　d.EEPROM

5. A field programmable ROM is called
   a. MROM　　b. PROM　　c. FROM　　d.FPROM

6. Program counter in a digital computer
   a. Counts the numbers of programs run in the machine.
   b. Counts the number of times a subroutine is called.
   c. Counts the number of times the loops are executed.
   d. Points the memory address of the next instruction to be fetched.

7. At the beginning of a fetch cycle, the contents of the program counter are
   a. incremented by one.　b. transferred to address bus.
   c. transferred to memory address register.　　d. transferred to memory data register.

8. Stack pointer is a -------- register
   　a. 16 bit　　b. 8 bit　　c. 32 bit　　d. 4bit

9. In memory mapped I/O device is identified by
   　a. 8bit address　b. IN instruction　　c. 16bit address　　d. OUT instruction

10. In I/O mapped input device is
    　a. latch　　b. buffer　　c. decoder　　d. stack

11. In I/O mapped output device is
    　a. buffer　　b. encoder　　c. latch　　d. stack

12. If accumulator content is 88H, after execution of CMA accumulator content will be—
    　a. 77H　　b. 93H　　c. FFH　　d. 80H

13. LDA is ---------
    　a. Instruction　b. arithmetic　c. logical branch　　d. data transfer

14. If A=56H,B=82H after execution of ANA B ,content of A= -----
    　a. 02H　　b. 56H　　c. 00H　　d. D8H

15. 8085 has EPROM of
    　a. 1Kb　　b. 526bytes　c. 64kb　　d. 256 bytes

16. In BCD to Binary Code Converter MS digit is multiplied by _____
    　a. 0A　b)0B　c)0C　d)0F

17. SID stands for
    　a. Serial input data　　b. Set interrupt Design
    　c. Serial interrupts device　　d. Set Input Data

18. ISR means
    　a. Interrupt service routine　　b. input service routine
    　c. input set register　　d. interrupt set register

19. TRAP, RST5.5, RST6.5, RST7.5 are ____
    　a)Hardware interrupts　b. software interrupts c. registers d. insulators

20. 2k static RAM memory cells organized as ___
    　a. 256 bytes　　b. 156 bytes　c. 56 bytes　　d. 16 bytes

(P.T.O)

21. The 8155 timer consist of two ___ registers
    a. 8 bit   b. 16 bit   c. 32 bit   d. 64 bit
22. The status register consist of ___ Latches.
    a. 7   b. 8   c. 5   d. 16
23. DAA command stands for _____
    a. Divide Accumulator Arithmetic   b. Decimal Accumulator Arithmetic
    c. Divide Adjust Accumulator   d. Decimal Adjust Accumulator
24. _____ is a tool that converts assembly language program to machine level language
    a. Accumulator   b. Debbuger   c. Assembler   d. Code Converter
25. The 8085 microprocessor has _____ hardware interrupts.
    a. 4   b. 5   c. 6   d. 7
26. _____ has highest priority among all interrupts
    a. RST 7.5   b. RST 6.5   c. INTR   d. TRAP
27. INTR interrupt is pin number _____ in pin diagram of 8085 microprocessor
    a. 7   b. 8   c. 9   d. 10
28. ISR address or Vector location for TRAP is
    a. 002C   b. 003C   c. 0024   d. 0034
29. The Pentium memory system is divided into
    a)4 banks   b)8 banks   c)6 banks   d)10 banks
30. Return CPU Identification code is carried out by the instruction
    a)CPUID   b)CPID   c)COPID   d)RCPID
31. The Pentium Pro microprocessor has provisions for a ----- address bus
    a)32 bit   c)64 bit   c)36 bit   63 bit
32. The---------instruction is used by external circuitry to request an interrupt.
    a)INRT   b)INTR   c)NIRT   d)NITR
33. The Pentium 4 and Core2 microprocessors require a modified ----------- and case to function properly in a system.
    a)AXT power supply b)TAX power supply c)ATX power supply d)XTA power supply
34. This significant advancement combines two microprocessors into a single package.   a)Hyper technology   b)Multi processor technology
    c) Combination technology   d)Hyper threading technology
35. A new feature added to the Pentium and Pentium Pro is the capability to check and generate
    a)purity   b)parity   c)errors   d)sum

Answer Sheet for Multiple Choice Questions

Q. No.	Ans.	Q. No.	Ans.	Q. No.	Ans.	Q. No.	Ans.	Q. No.	Ans.
1		8		15		22		29	
2		9		16		23		30	
3		10		17		24		31	
4		11		18		25		32	
5		12		19		26		33	
6		13		20		27		34	
7		14		21		28		35	

Marks Obtained: - _____   **Signature of the Examiner: -** _____